CLAIMS

WHAT IS CLAIMED IS:

1. A method of reducing the size of a translation lookaside buffer comprising utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer.

2. The method of Claim 1 wherein said bit corresponds to the least significant bit of said virtual page number.

3. The method of Claim 1 wherein said reading and writing is performed by way of using an existing translation lookaside buffer (TLB) control processor instruction set.

4. The method of Claim 3 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

5. The method of Claim 1 wherein said translation lookaside buffer of reduced size is compatible with one or more legacy systems utilizing any existing TLB instructions, software, or commands.

6. The method of Claim 1 wherein said virtual address comprises 32 bits.

7. The method of Claim 6 wherein said virtual page number is defined by bits [31:12] of said 32 bit virtual address.

8. The method of Claim 6 wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes.

9. The method of Claim 8 wherein said page mask size comprises 4 kilobytes.

10. The method of Claim 1 wherein said writing and reading is compatible with one or more existing TLB registers.

11. The method of Claim 10 wherein said one or more TLB registers comprises TLB registers defined by a MIPS architecture.

12. A method of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to consolidate even and odd page frame numbers into a single page frame number field of said translation lookaside buffer.

13. The method of Claim 12 wherein said bit corresponds to the least significant bit of said virtual page number.

14. The method of Claim 12 wherein said address translation of said translation look aside buffer is performed by way of using an existing control processor instruction set.

15. The method of Claim 12 wherein said consolidating even and odd page frame numbers into a single page frame number field implements a translation lookaside buffer of reduced size.

16. A system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers.

17. The system of Claim 16 wherein said buffer comprises a translation lookaside buffer of reduced size.

18. A system to provide virtual to physical memory address translation of a translation lookaside buffer comprising:

a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer.

19. The system of Claim 18 wherein using a single page frame number field implements a reduced size of said translation lookaside buffer.

20. The system of Claim 19 wherein said virtual to physical memory address translation is performed by way of using existing TLB control processor instructions.